IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended): A magnetic random access memory comprising:

a [[TMR]] tunnel magnetoresistive (TMR) element having first and second TMR layers stacked on each other; [[and]]

first and second current driving lines configured to generate magnetic fields for storing data to [[both]] each of said first and second TMR layers ~~individually~~, and to cross each other;

said first and second TMR layers are located between said first and second current driving lines; and

a value of a current of said first current driving line is greater than that of said second current driving line when data is written in said second TMR layer, and a value of a current of said second current driving line is greater than that of said first current driving line when data is written in said first TMR layer.

2. (Currently Amended): The magnetic random access memory according to claim 1, [[:]] further comprising:

a source line; and

a switching element connected between said TMR element and said source line, [[;]]

wherein said switch element turns on when data is read out from said TMR element.

3. (Currently Amended): The magnetic random access memory according to claim 1, [[:]]

wherein each of said first and second TMR layers has magnetic layers and [[a]] an insulating layer between said magnetic layers, and a direction of a spin of one of said magnetic layers is fixed by an antimagnetic layer.

4. (Currently Amended): The magnetic random access memory according to claim 3, [[:]]

wherein said TMR element has a nonmagnetic conductive layer provided between said first and second TMR layers.

5. (Currently Amended): The magnetic random access memory according to claim 3, [[:]]

wherein said antimagnetic layer is provided between said first and second TMR layers.

6. (Currently Amended): The magnetic random access memory according to claim 1, [[:]]

wherein the first current driving line is a bit line and said TMR element is in contact with said bit line.

7. (Currently Amended): The magnetic random access memory according to claim 6, [[:]]

wherein the second current driving line and the bit line are at right angles to each other.

8. (Currently Amended): The magnetic random access memory according to claim 7, [[:]]

wherein said TMR element is in contact with an under surface of said bit line and the second current driving line is provided ~~direct~~ directly under said TMR element.

9. (Currently Amended): The magnetic random access memory according to claim 7, [[:]]

wherein said TMR element is contact with an upper surface of said bit line and the second current driving line is provided direct upper said TMR element.

10. (Currently Amended): The magnetic random access memory according to claim 2, [[:]]

wherein the second current driving line and the source line are overlapped each other and extend [[to]] in the same direction.

11. (Currently Amended): The magnetic random access memory according to claim 3, [[:]]

wherein each of said first and second TMR layers stores data based on the direction of the spin of one of said magnetic layers.

12. (Currently Amended): The magnetic random access memory according to claim 1, [[:]]

wherein each of said first and second TMR layers receives a magnetic field intensity dependent on currents of said first and second current driving lines, as a result, the data is written in each of said first and second TMR layers individually.

13. (Currently Amended): The magnetic random access memory according to claim 12, [[:]]

wherein said first and second TMR layers are separated from each other.

14. (Currently Amended): The magnetic random access memory according to claim 1, [[:]]

wherein the asteroid curves of said first and second TMR layers are different from each other and the data is written in each of said first and second TMR layers individually.

15. (Currently Amended): The magnetic random access memory according to claim 14, [[:]]

wherein a data write operation begins with the first TMR layer and ends with the second TMR layer, and a strongest magnetic field intensity is required [[to]] for the first TMR layer to change the data and a weakest magnetic field intensity is required [[to]] for the second TMR layer to change the data.

16. (Currently Amended): The magnetic random access memory according to claim 1, [[:]]

wherein a current of the first current driving line flows [[at]] in only one direction and a current of the second current driving line flows [[at]] in one direction or another direction.

17. (Currently Amended): The magnetic random access memory according to claim [[1:]] 3,

wherein a thickness of said insulating layer ~~decides~~ determines a value of a resistance of each of said first and second TMR layers.

18. (Currently Amended): The magnetic random access memory according to claim 1, [[:]] further comprising:

a detecting resistance connected to said TMR element, [[;]]

wherein the data of said TMR element ~~detects~~ is detected based on a voltage of said detecting resistance in a read operation.

19. (Currently Amended): The magnetic random access memory according to claim 18, [[:]]

wherein said detecting resistance is provided at an outer portion [[out]] of a memory cell array portion.

20. (Currently Amended): The magnetic random access memory according to claim 18, [[:]] further comprising:

[[a]] the power source electrically connected to said TMR element in a read operation and ~~generated~~ generates a read current.

21. (Withdrawn): A magnetic random access memory comprising:

a first current driving line;

a second current driving line configured to cross said first current driving line;

a third current driving line configured to cross said first current driving line;

a first TMR element contacted to an under surface of the first current driving line;

a first switching element connected to said first TMR element;

a second TMR element contacted to an upper surface of the first current driving line; and

a second switching element connected to said second TMR element;

wherein each of said first and second TMR elements has first and second TMR layers stacked each other, the first and second current driving lines configure to generate magnetic fields for storing data to both of said first and second TMR layers of the first TMR element individually, and the first and third current driving lines configure to generate magnetic fields for storing data to both of said first and second TMR layers of the second TMR element individually.

22. (Withdrawn): The magnetic random access memory according to claim 21:

wherein each of said first and second TMR layers includes magnetic layers and a insulating layer between said magnetic layers.

23. (Withdrawn): The magnetic random access memory according to claim 21:

wherein each of the first and second TMR elements has a nonmagnetic conductive layer between said first and second TMR layers.

24. (Withdrawn): The magnetic random access memory according to claim 21:

wherein said first current driving line is a bit line, said second current driving line is provided direct under said first TMR element, and said third current driving line is provided direct upper said second TMR element.

25. (Withdrawn): The magnetic random access memory according to claim 24:

wherein the second and third current driving lines are at right angles to said bit line.

26. (Withdrawn): The magnetic random access memory according to claim 21:

wherein currents of the first and second current driving lines generate magnetic fields for writing data to said first TMR element.

27. (Withdrawn): The magnetic random access memory according to claim 21:

wherein currents of the first and third current driving lines generate magnetic fields for writing data to said second TMR element.

28. (Withdrawn): The magnetic random access memory according to claim 21:

wherein source terminals of the first and second switching elements are electrically connected a source line.

29. (Withdrawn): The magnetic random access memory according to claim 28:

wherein the second and third current driving lines are overlapped each other and extends same direction.

30. (Withdrawn): The magnetic random access memory according to claim 29:

wherein the source line is overlapped with the second and third current driving lines.

31. (Withdrawn): A magnetic random access memory comprising:

a first current driving line;

first and second TMR elements contacted to said first current driving line and each of said first and second TMR elements has first and second TMR layers stacked each other; and

a switching element connected to said first and second TMR elements;

wherein said first current driving line configures to generate magnetic fields for storing data to both of said first and second TMR layers individually.

32. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the first TMR element is contacted to an under surface of said first current driving line and the second TMR element is contacted to an upper surface of said first current driving line.

33. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the first and second TMR elements are contacted to an under surface of said first current driving line.

34. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the first and second TMR elements are contacted to an upper surface of said first current driving line.

35. (Withdrawn): The magnetic random access memory according to claim 31:

wherein each of said first and second TMR layers has magnetic layers and a insulating layer between said magnetic layers.

36. (Withdrawn): The magnetic random access memory according to claim 31:

wherein each of said first and second TMR elements has a nonmagnetic conductive layer between said first and second TMR layers.

37. (Withdrawn): The magnetic random access memory according to claim 31:

wherein said first current driving line comprises a first bit line and a second bit line above said first bit line, and the first and second bit lines are electrically connected each other.

38. (Withdrawn): The magnetic random access memory according to claim 37:

wherein the first TMR element is connected to said first bit line and the second TMR element is connected to said second bit line.

39. (Withdrawn): The magnetic random access memory according to claim 37:

wherein the first and second bit lines are electrically connected each other at an end portion of a memory cell array.

40. (Withdrawn): The magnetic random access memory according to claim 37:

further comprising

a second current driving line near to the first TMR element; and

a third current driving line near to the second TMR element.

41. (Withdrawn): The magnetic random access memory according to claim 40:

wherein the first TMR element is provided between the second current driving line and the first bit line, and the second TMR element is provided between the third current driving line and the second bit line.

42. (Withdrawn): The magnetic random access memory according to claim 41:

wherein the second and third current driving lines are at right angles to the first and second bit lines.

43. (Withdrawn): The magnetic random access memory according to claim 42:

wherein currents of the second current driving line and the first bit line generate magnetic fields for writing data to said first TMR element.

44. (Withdrawn): The magnetic random access memory according to claim 42:

wherein currents of the third current driving line and the second bit line generate magnetic fields for writing data to said second TMR element.

45. (Withdrawn): The magnetic random access memory according to claim 42:

wherein one of the second and third current driving lines is provided between the first bit line and the second bit line.

46. (Withdrawn): The magnetic random access memory according to claim 31:

further comprising

a detecting resistance connected to the first current driving line;

wherein data of the first and second TMR elements detect based on a voltage of said detecting resistance in a read operation.

47. (Withdrawn): The magnetic random access memory according to claim 46:

wherein said detecting resistance is provided at an outer portion out of a memory cell array portion.

48. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the data of the first TMR element is equal to a write data, when the data of the first TMR element after a write operation is equals to the data of the first TMR element before the write operation.

49. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the data of the first TMR element is different from a write data, when the data of the first TMR element after a write operation is different from the data of the first TMR element before the write operation.

50. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the data of the second TMR element is equal to a write data, when the data of the second TMR element after a write operation is equals to the data of the second TMR element before the write operation.

51. (Withdrawn): The magnetic random access memory according to claim 31:

wherein the data of the second TMR element is different from a write data, when the data of the second TMR element after a write operation is different from the data of the second TMR element before the write operation.

52. (Withdrawn): The magnetic random access memory according to claim 31:

wherein a write operation is executed to the first TMR element after data of the first TMR element is read.

53. (Withdrawn): The magnetic random access memory according to claim 31:

wherein a write operation is executed to the second TMR element after data of the first TMR element is read.

54. (Currently Amended): The magnetic random access memory according to claim 1, [[:]] further comprising:

a register temporarily ~~latched~~ latches the data having a plurality of bits.

55. (Withdrawn): The magnetic random access memory according to claim 21: further comprising

a register temporarily latched data having a plurality of bits.

56. (Withdrawn): The magnetic random access memory according to claim 31: further comprising

a register temporarily latched data having a plurality of bits.